14. (Amended) The voltage controlled oscillator of Claim 13, further comprising an additional delay unit.

15. (Amended) The voltage controlled oscillator of Claim 7, wherein in the first delay unit and in the second delay unit, drains of the first amplifier are connected to drains of the second amplifier, said connections forming output terminals.

16. (Amended) The voltage controlled oscillator of Claim 15, further comprising an additional delay unit.

REMARKS

1. The application was filed with 23 claims. Claims 1 and 10-16 have been amended. Claims 1-23 are pending in the application. Reconsideration by the Examiner of the claims still pending is respectfully requested. Applicant thanks the Examiner for finding allowable subject matter in Claim 18 if rewritten in independent format with all the limitations of the base claim and all intervening claims.

2. The Examiner has required a restriction as between Invention I, Claims 1-19, drawn to a subcombination, and Invention II, Claims 20-23, drawn to a combination. Applicant elects Invention I, Claims 1-19 and traverses the requirement, per the telephone conversation of June 5, 2002. The combination as claimed, in Claims 20-23, does require the particular VCO having at least two delay units, each delay unit comprising only four transistors. Therefore, the inventions are not distinct and the restriction is improper. The Examiner is respectfully requested to withdraw the restriction requirement and examine Claims 20-23, as well as Claims 1-19.

3. The Examiner has rejected claims 15-17 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Claim 15 incorrectly states that the drains of the first amplifier are connected to the sources of the second amplifier. At least Figs. 5-6 clearly depict drains of the first amplifier connected to drains of the second amplifier. Claim 15 has been amended. Accordingly, Applicant believes the Examiner's rejections of Claims 15-17 under 35 U.S.C. § 112, second paragraph, are overcome, and respectfully requests the Examiner to withdraw the rejections.

4. The Examiner has rejected claims 1-3 and 10-17 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Claim 1 incorrectly states that a control input and power supply voltage are connected to the drains of the first amplifier, while at least Figs. 3A, 3B and 5 depict a control input and power supply voltage connected to the sources of the first amplifier. Claim 1 has been amended. Applicant submits that Claims 1-3 have thus been corrected.

Claims 10-16 contain unnecessary limitations concerning the connections of additional delay units. Claims 10-16 have been amended, and through these amendments, dependent Claim 17. Accordingly, Applicant believes the Examiner's rejections of Claims 10-17 under 35 U.S.C. § 112, second paragraph, are overcome. Applicant respectfully requests the Examiner to withdraw the rejections of Claims 1-3 and 12-17 under 35 U.S.C. § 112.

5. The Examiner has rejected claims 1 and 4-6 under 35 U.S.C. § 102 (b) as being anticipated by U.S. Pat. No. 6,100,659, to An et al. ("An"). The Examiner states that An discloses in Fig. 7 a circuit comprising a first amplifier having a first (MN6) and a second (MN7) transistor connected as a two-transistor positive amplifier. Fig. 7 of An, however, discloses a four-transistor positive amplifier that includes MN5-MN8. An, therefore, does not disclose a two-transistor positive amplifier. Since An does not disclose a two-transistor positive amplifier, An does not anticipate the claimed invention. An invention is not anticipated when the same device or method, including all the

limitations contained in the claims, is not described in a single prior art reference.[1] Accordingly, the Examiner is requested to withdraw the rejection of Claims 1 and 4-6 under 35 U.S.C. § 102 (b) based on An.

6. The Examiner has rejected claims 1-4 under 35 U.S.C. § 102 (b) as being anticipated by U.S. Pat. No. 6,218,892, to Soumyanath et al. ("Soumyanath"). The Examiner states that Soumyanath's Fig. 14 discloses a first amplifier having a first (M11) and second (M12) transistor connected as a two–transistor positive amplifier. Figure 14, however, discloses a four-transistor amplifier, including M10, M11, M12 and M13, not a two-transistor amplifier.

Soumyanath, therefore, does not disclose a two-transistor positive amplifier. Since Soumyanath does not disclose a two-transistor positive amplifier, Soumyanath does not anticipate the claimed invention. An invention is not anticipated when the same device or method, including all the limitations contained in the claims, is not described in a single prior art reference.[2] Accordingly, the Examiner is requested to withdraw the rejection of Claims 1-4 under 35 U.S.C. § 102 (b) based on Soumyanath.

7. The Examiner has rejected Claims 1-7 and 7-14 under 35 U.S.C. § 102(e), as being anticipated by U.S. Pat. No. 6,377,511, Okuda et al. ("Okuda"). The Examiner states that Fig. 8 of Okuda discloses a circuit comprising a first amplifier having a first (Q5) and a second (Q6) transistor connected as a two-transistor positive amplifier, as claimed in independent Claims 1 and 7 of the present invention. Fig. 8 of Okuda, however, discloses not a two-transistor amplifier, but a four-transistor positive amplifier, including transistors Q3, Q4, Q5 and Q6. Okuda, therefore, does not disclose a two-transistor positive amplifier. Since Okuda does not disclose a two-transistor positive amplifier, Okuda does not anticipate the claimed invention. Accordingly, the Examiner is requested to withdraw the rejection of Claims 1-4 and 7-14 under 35 U.S.C. § 102 (b) based on Okuda.

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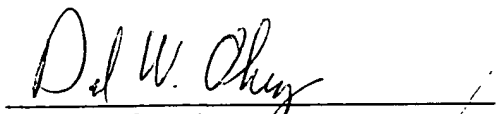
[1] Ex Parte Levy, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. Appl. & Int. 1990).
[2] Id.

8. Applicant has responded to the Restriction requirement by the Examiner by electing Invention I and traversing the restriction. Applicant again thanks the Examiner for finding potentially patentable subject matter in the present application, if Claim 18 is rewritten in independent format with all its limitations and those of its base claim and all intervening claims. Applicant requests that the Examiner enter the Amendments and reconsider the application. Applicant respectfully requests that the Examiner withdraw the rejections for indefiniteness and anticipation and advance the application to allowance.

Respectfully submitted,



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APPENDIX A

1. (Amended) A differential controlled delay unit, comprising:

a first amplifier having a first and a second transistor connected as a two-transistor positive amplifier, wherein a gate of the first transistor is connected to a drain of the second transistor and a gate of the second transistor is connected to a drain of the first transistor; and

a second amplifier having a third and a fourth transistor, a drain of the third and fourth transistors connected to a drain of the first and second transistors to form output terminals, wherein a differential input voltage is connected to gates of the second amplifier transistors, and a control input and power supply voltage is connected to [drains] sources of the first amplifier.

10. (Amended) The voltage controlled oscillator of Claim 7, further comprising an additional delay unit[, wherein output signals from the second delay unit are connected to gates of the additional delay unit, and output signals of the additional delay unit are connected to gates of the first delay unit].

11. (Amended) The voltage controlled oscillator of Claim 7, wherein the transistors for the first amplifiers are PMOS and the transistors for the second amplifiers are NMOS and a drain of the first and second transistors is connected to a drain of the third and fourth transistors to form outputs of the delay units[,

and wherein outputs of the first delay unit are connected to gates of the second delay unit, and outputs of the second delay unit are connected to gates of the first delay unit, and wherein a control input and power supply voltage is connected to sources of the second amplifiers].

12. (Amended) The voltage controlled oscillator of Claim 11, further comprising an additional delay unit[, wherein outputs from the second delay unit are connected to gates of the additional delay unit, and outputs of the additional delay unit are connected to gates of the first delay unit].

13. (Amended) The voltage controlled oscillator of Claim 7, wherein in the first delay unit and the second delay unit, drains of the first amplifier are connected to drains of the second amplifier to form output terminals[,

and wherein the output signals of the first delay unit are connected to gates of the second delay unit, and output signals of the second delay unit are connected to gates of the first delay unit, and wherein a control input and power supply voltage is connected to sources of the first and second delay units].

14. (Amended) The voltage controlled oscillator of Claim 13, further comprising an additional delay unit[, wherein output signals from the second delay unit are connected to gates of the additional delay unit, and output signals of the additional delay unit are connected to gates of the first delay unit].

15. (Amended) The voltage controlled oscillator of Claim 7, wherein in the first delay unit and in the second delay unit, drains of the first amplifier are connected to [sources] <u>drains</u> of the second amplifier, said connections forming output terminals[,

and wherein output terminals of the first delay unit are connected to gates of the second delay unit, and output terminals of the second delay unit are connected to gates of the first delay unit].

16. (Amended) The voltage controlled oscillator of Claim 15, further comprising an additional delay unit[, wherein output signals from the second delay unit are connected to gates of the additional delay unit, and output signals of the additional delay unit are connected to gates of the first input unit].